Amendments to the Claims:

The below listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (previously presented) A CAM (content addressable memory) apparatus comprising:

a first memory device with a word line input and at least one storage node for storing a first bit of a data word;

a second memory device with a word line input and at least one storage node for storing a second bit of a data word; and

a comparator device for comparing the first and second stored bits with first and second precoded comparison bits fed via four inputs and for driving a hit node in the event of the first stored bit corresponding to the first comparison bit and the second stored bit corresponding to the second comparison bit.

2. (currently amended) The CAM apparatus according to Claim [[1,]]14 wherein the comparator device has four signal paths each having three transistors between a supply voltage and the hit node.

3. (currently amended) The CAM apparatus according to Claim [[2,]]19, wherein the comparator device has a series-parallel circuit comprising twelve field-effect transistors of a first conduction type.

4. (previously presented) The CAM apparatus according to Claim 3, wherein the comparator device has four parallel-connected series circuits comprising in each case three field-effect transistors of the first conduction type.

5. (currently amended) The CAM apparatus according to Claim [[2,]]19, wherein the comparator device has a series-parallel circuit comprising eight field-effect transistors of a first conduction type.

6. (currently amended) The CAM apparatus according to Claim [[2,]]19, wherein a first, second, third and fourth storage node of the memory devices are connected to gate terminals of a first and second field-effect transistor of the first conduction type of a respective path of a series-parallel circuit in such a way that precisely one path can be switched through by each of the four bit combinations possible from two bits.

7. (previously presented) The CAM apparatus according to Claim 6, wherein a respective third transistor of each one of the four paths is connected, on the gate side, to a respective one of the four inputs for inputting the first and second precoded comparison bits.

8. (previously presented) The CAM apparatus according to Claim 3, wherein the comparator device has a field-effect transistor of a second conduction type which differs from the first conduction type, the field-effect transistor having a control terminal and located between the hit node and a reference potential.

9. (previously presented) The CAM apparatus according to Claim 8, wherein the four input lines comprise four comparison lines and the field-effect transistor (N; P) of the second conduction type can be switched through via the control terminal if all of the comparison lines have a predetermined signal level.

10. (previously presented) The CAM apparatus according to Claim 3, wherein the comparator device has four series-connected field-effect transistors of a second conduction type, which differs from the first conduction type.

11. (previously presented) The CAM apparatus according to Claim 10, wherein the four field-effect transistors of the second conduction type are connected in series with a series-

parallel circuit comprising field-effect transistors of the first conduction type between the hit node and a reference potential.

12. (previously presented) The CAM apparatus according to Claim 3, wherein the field-effect transistors of the first conduction type form a p channel and the field-effect transistors of the second conduction type form an n channel.

13. (previously presented) The CAM apparatus according to Claim 3, wherein the field-effect transistors of the first conduction type form an n channel and the field-effect transistors of the second conduction type form a p channel.

14. (previously presented) The CAM apparatus according to Claim 1, wherein the comparator device has a holding device for maintaining a signal level at the hit node.

15. (currently amended) The CAM apparatus according to Claim [[14,]]2, wherein the holding device has three transistors, of which a first transistor of the three transistors and a second transistor of the three transistors forms an inverter the input of which is connected to the hit node and the output of which is connected to a gate of a third transistor of the three transistors.

16. (currently amended) The CAM apparatus according to Claim [[1,]]2, wherein a circuit that is upstream of the CAM apparatus generates the two precoded comparison bits and can be operated statically or dynamically.

17. (currently amended) The CAM apparatus according to Claim [[1,]]2, wherein both a downstream series pass gate hit path and a wired-Or hit path can be driven via the hit node.

18. (currently amended) The CAM apparatus according to Claim 1, wherein the memory devices are in each case constructed identically and in each case have six transistors, four of which form two antiparallel inverters ~~(I)~~.

19. (new) A CAM (content addressable memory) apparatus comprising:

a first memory device with a word line input and at least one storage node for storing a first bit of a data word;

a second memory device with a word line input and at least one storage node for storing a second bit of a data word; and

a comparator device for comparing the first and second stored bits with first and second precoded comparison bits fed via four inputs and for driving a hit node in the event of the first stored bit corresponding to the first comparison bit and the second stored bit corresponding to the second comparison bit;

wherein the comparator device has four signal paths each having three transistors between a supply voltage and the hit node.

20. (new) A CAM (content addressable memory) apparatus comprising:

a first memory device with a word line input and at least one storage node for storing a first bit of a data word;

a second memory device with a word line input and at least one storage node for storing a second bit of a data word; and

a comparator device for comparing the first and second stored bits with first and second precoded comparison bits fed via four inputs and for driving a hit node in the event of the first stored bit corresponding to the first comparison bit and the second stored bit corresponding to the second comparison bit,

wherein the comparator device has a holding device for maintaining a signal level at the hit node,

wherein the holding device has three transistors, of which a first transistor and a second transistor form an inverter, the input of which is connected to the hit node and the output of which is connected to a gate of a third transistor of the three transistors.

21. (new) A CAM (content addressable memory) apparatus comprising:

a first memory device with a word line input and at least one storage node for storing a first bit of a data word;

a second memory device with a word line input and at least one storage node for storing a second bit of a data word; and

a comparator device for comparing the first and second stored bits with first and second precoded comparison bits fed via four inputs and for driving a hit node in the event of the first stored bit corresponding to the first comparison bit and the second stored bit corresponding to the second comparison bit;

wherein a circuit that is upstream of the CAM apparatus generates the two precoded comparison bits and can be operated statically or dynamically.

22. (new) A CAM (content addressable memory) apparatus comprising:

a first memory device with a word line input and at least one storage node for storing a first bit of a data word;

a second memory device with a word line input and at least one storage node for storing a second bit of a data word; and

a comparator device for comparing the first and second stored bits with first and second precoded comparison bits fed via four inputs and for driving a hit node in the event of the first stored bit corresponding to the first comparison bit and the second stored bit corresponding to the second comparison bit;

wherein both a downstream series pass gate hit path and a wired-Or hit path can be driven via the hit node.